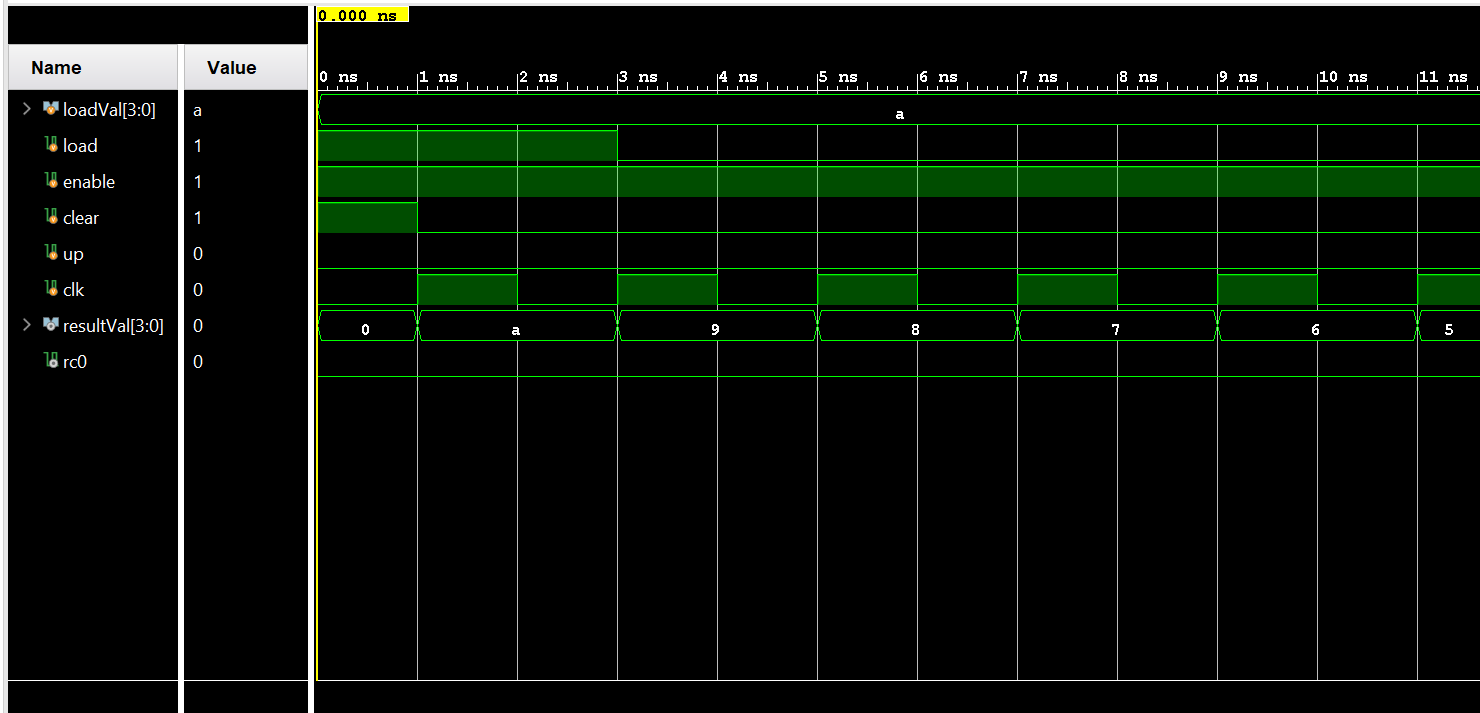
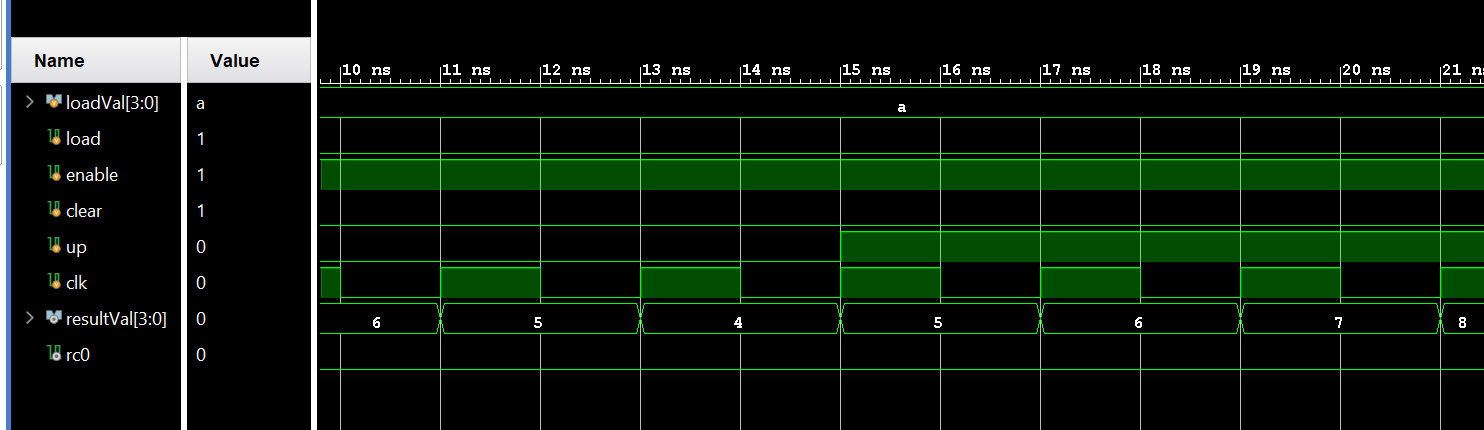
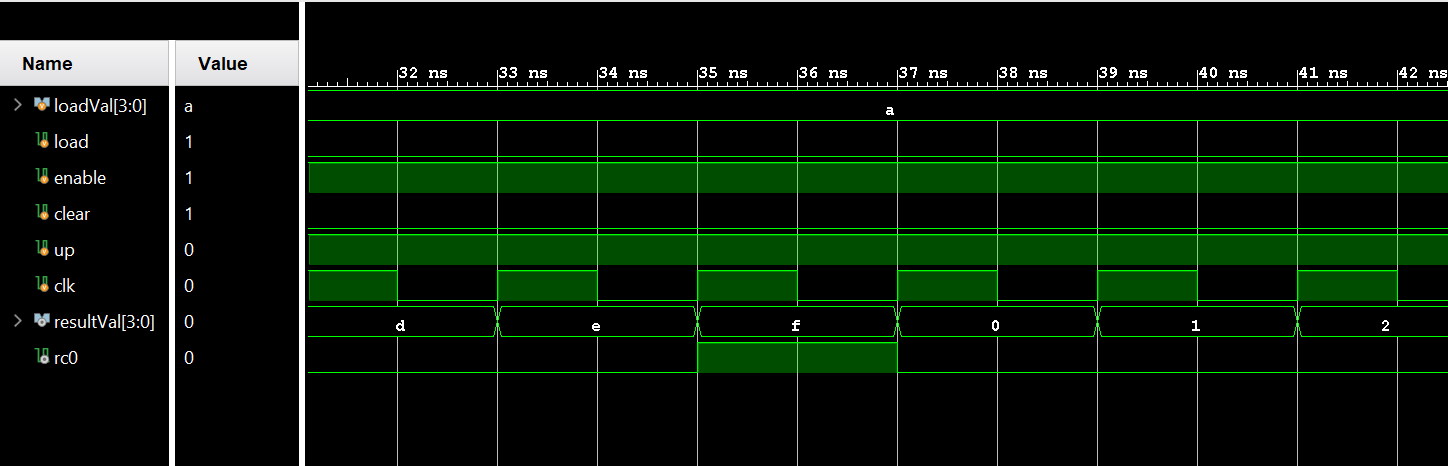
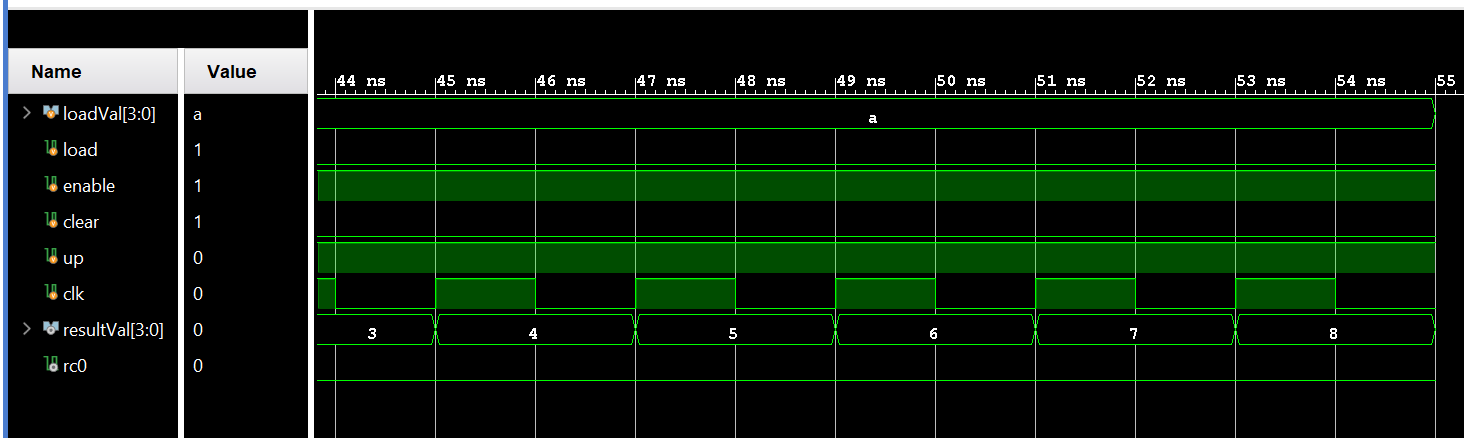
**Question 5:**

No special use cases. First testbench loads 10, counts down to 4 (6 cycles) and up 20 times









In Part 2, an 8-bit counter is built from the 2 4-bit counter instances. It loads 122 and counts down 124 times. The enable of the 2nd counter (Higher 4 bits) is triggered in the following cases:

1) When counting up or down, if RC0 of the lower counter is on (lower counter output = F and Up = 1 or 0 and Up = 0)

2) When loading an 8-bit number into the counter. Due to technical issues, load is incorporated into the ENABLE sensitivity list.

